In the Claims

CLAIMS

1. (Previously Amended) Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer, the high K substantially amorphous material and the high K substantially crystalline material constituting different chemical compositions, the high K substantially crystalline material being received over the high K substantially amorphous material; and

wherein the high K substantially crystalline material layer is at least 70% crystalline and less than 90% crystalline.

Claims 2 and 3 (Previously Cancelled).

4. (Original) The integrated circuitry of claim 1 wherein at least one of the first and second electrodes comprises elemental metal, metal alloy, conductive metal oxides, or mixtures thereof.

5. (Original) The integrated circuitry of claim 1 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

6. (Original) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

7. (Original) The integrated circuitry of claim 6 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode and the second capacitor electrode.

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8. (Original) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrodes and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrodes.

9. (Original) The integrated circuitry of claim 1 wherein the high K capacitor dielectric region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.

10. (Previously Amended) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 98% amorphous.

11. (Previously Amended) The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially amorphous material layer being received between the semiconductor substrate and the high K substantially crystalline material layer.

12. (Original) The integrated circuitry of claim 11 wherein the semiconductor substrate comprises bulk monocrystalline silicon.

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13. (Original) The integrated circuitry of claim 11 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

14. (Original) The integrated circuitry of claim 11 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

Claims 15-55 (Previously Cancelled).

56. (Previously Added) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 70% amorphous.

57. (Previously Added) The integrated circuitry of claim 1 further comprising a substrate supporting the first and second capacitor electrodes, and an insulative layer intermediate the substrate and the first and second capacitor electrodes.

58. (Previously Added) The integrated circuitry of claim 57 wherein the insulative layer comprises an oxide layer.

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59. (Previously Added) The integrated circuitry of claim 57 wherein the insulative layer comprises silicon dioxide.

60. (Previously Added) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer comprises a thickness in a range of about 20 Ångstroms to about 250 Ångstroms.

61. (Previously Added) The integrated circuitry of claim 1 wherein the high K substantially crystalline material layer comprises a thickness in a range of about 20 Ångstroms to about 90 Ångstroms.

62. (Previously Added) The integrated circuitry of claim 1 wherein the high K capacitor dielectric region comprises a thickness in a range of about 40 Ångstroms to about 500 Ångstroms.

63. (Currently Amended) Integrated circuitry comprising:

a substrate having an upper surface;

at least two gate structures laterally spaced from one another and formed over the upper surface of the substrate, the two gate structures having uppermost surfaces;

insulative material formed over the two gate structures and the upper surface of the substrate;

an opening formed in the insulative material between the two gate structures; and

a capacitor comprising:

a first electrode layer formed within the opening and having a portion most proximate and spaced from the upper surface of the substrate, the portion elevationally below the uppermost surfaces of the two gate structures;

a high K dielectric layer formed over the first electrode layer and within the opening, the high K dielectric layer comprising material other than ferroelectric material; and

a second electrode layer formed over the high K dielectric layer.

64. (Previously Added) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising crystalline material.

65. (Previously Added) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising amorphous material.

66. (Previously Added) The integrated circuitry of claim 63 wherein the high K dielectric layer comprises a portion of amorphous material and a portion of crystalline material.

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67. (Previously Added) The integrated circuitry of claim 63 wherein the high K dielectric layer comprises an amorphous layer adjacent the first electrode layer and a crystalline layer adjacent the second electrode layer.

68. (Previously Added) The integrated circuitry of claim 63 wherein the high K dielectric layer comprises a crystalline layer adjacent the first electrode layer and an amorphous layer adjacent the second electrode layer.

69. (Previously Amended) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising greater than 70% and less than or equal to 98% crystalline material.

70. (Previously Amended) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising greater than 70% and less than or equal to 98% amorphous material.

71. (Previously Added) The integrated circuitry of claim 63 wherein the opening comprises a trench.

72. (Previously Added) The integrated circuitry of claim 63 wherein the second electrode layer is formed within the opening.

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73. (Previously Added) The integrated circuitry of claim 63 further comprising a conductive region intermediate the first electrode layer and substrate, the conductive region electrically connecting the first electrode layer and substrate.

74. (Previously Added) The integrated circuitry of claim 73 wherein the conductive region comprises conductive polysilicon.

75. (Previously Added) The integrated circuitry of claim 73 wherein the conductive region comprises a metal.

76. (Previously Added) The integrated circuitry of claim 73 wherein the conductive region comprises a metal compound and a conductive barrier layer material.

77. (Previously Added) The integrated circuitry of claim 73 wherein the conductive region comprises a material different than material of the first electrode layer.

78. (Previously Added) The integrated circuitry of claim 73 wherein the first electrode layer comprises a monolithic unitary material.

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79. (Previously Added) The integrated circuitry of claim 63 wherein the first electrode layer comprises conductively doped polysilicon.

80. (Previously Added) The integrated circuitry of claim 1 wherein the high K substantially crystalline material layer is less than 80% crystalline.

81. (New) The integrated circuitry of claim 1 wherein the integrated circuitry is formed over a semiconductor-on-insulative substrate.

82. (New) The integrated circuitry of claim 63 wherein the substrate comprises a semiconductor-on-insulative substrate.

83. (New) Integrated circuitry comprising:

a substrate having insulative material formed over the substrate;

an opening formed in the insulative material; and

a capacitor comprising:

a first electrode layer formed within the opening;

a high K dielectric layer formed over the first electrode layer and within the opening; and

a second electrode layer formed over the high K dielectric layer; and

wherein the high K dielectric layer comprises a portion of amorphous material and a portion of crystalline material.

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84. (New) The integrated circuitry of claim 83 wherein the portion of crystalline material comprises at least 70% crystalline and less than 90% crystalline.

85. (New) The integrated circuitry of claim 83 wherein the portion of crystalline material is equal to about 70% crystalline.

86. (New) The integrated circuitry of claim 83 wherein the portion of amorphous material comprises at least 70% amorphous phase.

87. (New) The integrated circuitry of claim 83 wherein the high K dielectric layer comprises Ta_2O_5.

88. (New) The integrated circuitry of claim 83 wherein the portion of amorphous material comprises greater than 90% amorphous phase.

89. (New) The integrated circuitry of claim 83 wherein the portion of amorphous material comprises material different from material of the portion of crystalline material.